

10/647602

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,798,641 B1
DATED : September 28, 2004
INVENTOR(S) : Peter J. Hopper et al.

Page 1 of 3

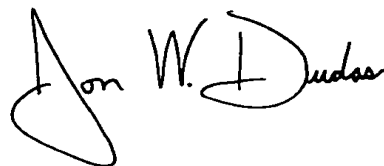
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page illustrating a figure should be deleted, and substituted therefor title page illustrating a figure. (Attached)

Delete Fig 1, and substitute therefor Fig 1. (Attached)

Signed and Sealed this

Fifth Day of April, 2005

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Hopper et al.

(10) Patent No.: **US 6,798,641 B1**
(45) Date of Patent: **Sep. 28, 2004**

(54) **LOW COST, HIGH DENSITY DIFFUSION
DIODE-CAPACITOR**

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/647,602**

(22) Filed: **Aug. 25, 2003**

(51) Int. Cl.⁷ **H01G 4/228**

(52) U.S. Cl. **361/306.1; 361/306.3;**
361/321.1; 361/321.4; 361/311; 361/313;
361/303

(58) Field of Search **361/306.1, 306.3,**
361/321.1, 321.4, 303, 305, 311, 313, 301.2;
438/253, 254, 397, 398; 257/306, 355,
359, 362

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,355,014 A • 10/1994 Rao et al. 257/533
6,190,964 B1 • 2/2001 Winters 438/254

* cited by examiner

Primary Examiner—Dean A. Reichard

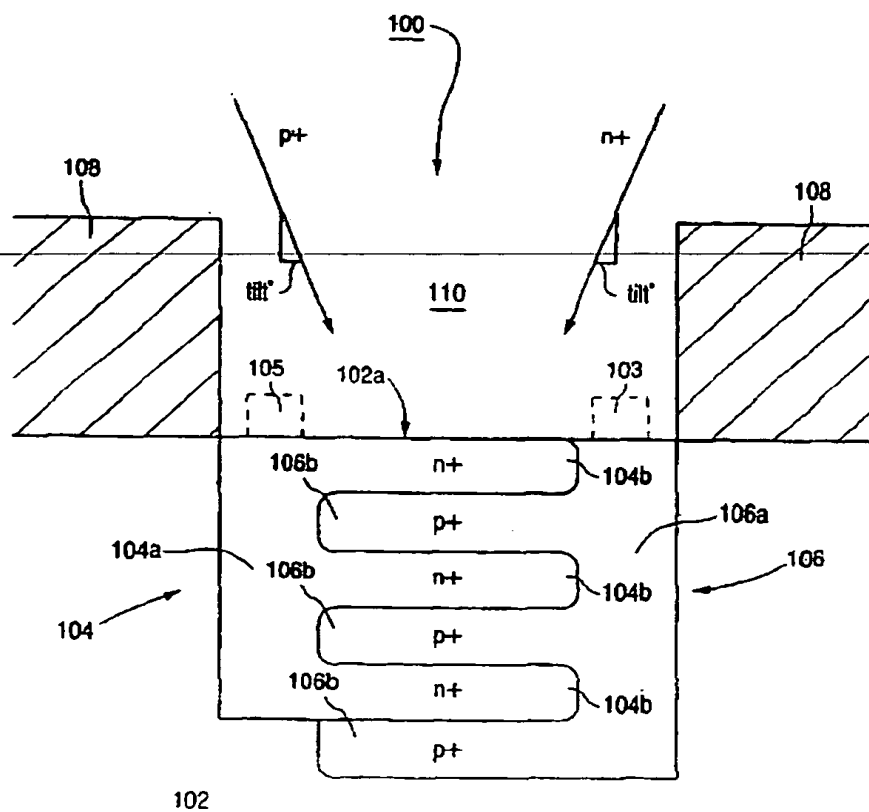
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(57) **ABSTRACT**

A multiple-layer diffusion junction capacitor structure includes multiple layers of inter-digitated P-type dopant and N-type dopant formed in a semiconductor substrate. An opening in a hard mask is formed taking care to control the angle of the sidewall using a dry, anisotropic etching process. P-type and N-type dopant are then implanted at positive and negative shallow angles, respectively, each with a different energy and dose. By utilizing the properly determined implant angles, implant energies and implant doses for each of the dopant types, a high capacitance and high density diode junction capacitor, with inter-digitated N-type and P-type regions in the vertical direction is provided.

6 Claims, 1 Drawing Sheet



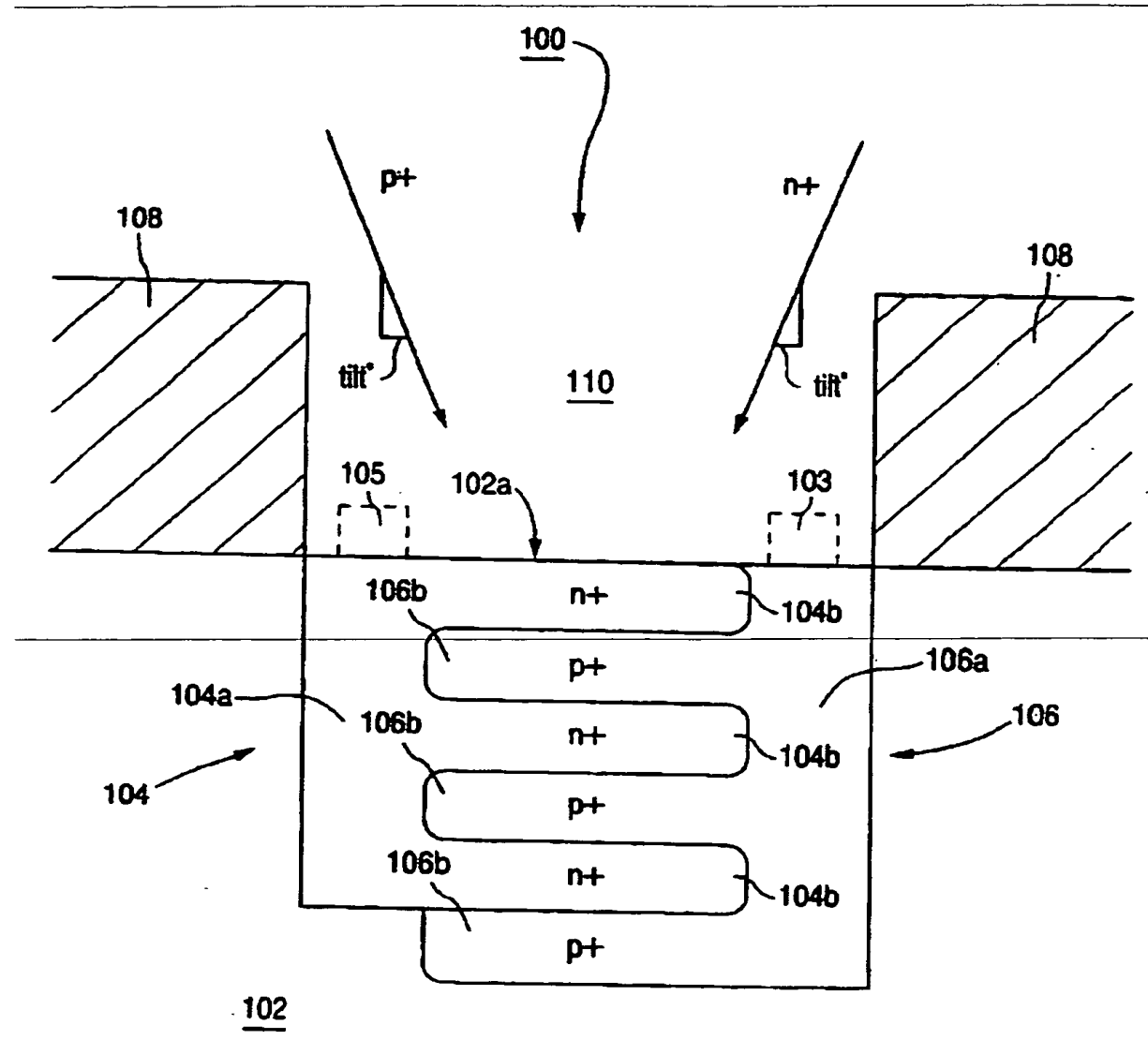


FIG. 1